Amendments to the Specification:

On page 6, lines 4-13, please amend the paragraph as follows:

A SBox92 (S92) operator 350 generates a 9-bit signal y0, y1, . . ., y8 from the signal RL_2 by Eq. (1). A ZE2 unit 360 receives the signal ~~RR_1~~ RR_2, adds two zeroes to the MSB of the signal ~~RR_1~~ RR_2, and outputs a 9-bit signal. An Exclusive-OR operation is performed to logically "exclusive OR" the outputs of the S92 operator 350 and the ZE2 unit 360 to provide a 9-bit signal RL_3. A TR2 unit 370 removes two zero bits from the MSBs of the 9-bit signal RL_3. A SBox72 (S72) operator 380 generates a 7-bit signal y0, y1, . . ., y6 from the input signal RR_2 (=RR_3) using Eq. (2). Another Exclusive-OR operation is performed to logically "exclusive OR" the outputs of the TR2 370 and the S72 operator 380 to provide a 7-bit signal RR_4.

On page 12, lines 9-30, please amend the paragraph as follows:

The 32-bit signal R_0 which was divided from the 64-bit signal in FIG. 4 is further divided into a 16-bit signal $L_{0'}$ and a 16-bit signal $R_{0'}$ in the FO2 cipher 502. A signal L_6 is generated by performing a logical exclusive-OR operation on the signal $L_{0'}$ using the 16-bit signal L_5. Meanwhile, a signal R_4 is generated by performing a logical exclusive-OR operation on the signal $R_{0'}$ using the 16-bit signal R_3. A signal R_5 is generated by performing a logical exclusive-OR operation on the signal R_4 using a sub-encryption key $KO_{2,1}$. An $Fl_{2,1}$ sub-cipher 514 generates a signal R_{5D} by encrypting the signal R_5 with a sub-encryption key $KI_{2,1}$. A signal R_6 is generated by performing a logical exclusive-OR operation on the signals R_{5D} and L_6. That is, the $Fl_{1,3}$ sub-cipher 513 and the $Fl_{2,1}$ sub-cipher 514 synchronize the signal L_6 to the signal R_6 without using delays. A signal L_7 is generated by performing a logical exclusive-OR operation on the signal L_6 with a 16-bit sub-encryption key $KO_{2,2}$. An ~~$FL_{2,2}$~~ $Fl_{2,2}$ sub-cipher 515 generates a signal L_{7D} by encrypting the signal L_7 with a 16-bit sub-encryption key $KI_{2,2}$. A delay (D8) 640 delays the signal R_6 and outputs a delayed signal R_{6D}. A signal L_8 is generated by performing a logical exclusive-OR operation on the signals L_{7D} and R_{6D}. A signal R_7 is generated by performing a logical exclusive-OR operation on the signal R_6 with a 16-bit sub-encryption key $KO_{2,3}$. An $Fl_{2,3}$ sub-cipher 516 generates a signal R_{7D} by encrypting the signal R_7 with a 16-bit sub-encryption key $KI_{2,3}$. A signal R_8 is generated by performing a logical exclusive-OR operation on the signals R_{7D} and L_8. Consequently, a 32-bit ciphertext $L_8||R_8$ is generated by operating the 16-bit signal L_8 with the 16-bit signal R_8.

On page 13, line 22 – page 14, line 9, please amend the paragraph as follows:

That is, the S91 operator 710 generates the 9-bit signal ~~y1~~y0, y2, . . ., y8 by performing parallel logical AND operations and then performing a logical exclusive-OR operation of a 9-bit signal x0, x1, . . ., x8 in parallel. A ZE1 unit 720 receives the signal RR_0, adds two zeroes to the MSB of the signal RR_0, and outputs a 9-bit signal. An Exclusive-OR operation is performed to logically "exclusive OR" the outputs of the S91 operator 710 and the ZE1 unit 720 to provide a 9-bit signal RL_1. Another Exclusive-OR operation is performed to logically "exclusive OR" the signal RL_1 and a 9-bit sub-encryption key $KI_{1,1,2}$, to provide a 9-bit signal RL_2. The signal RL_2 is temporarily stored in a first register (register 1) 800.

On page 14, line 17 – page 15, line 4, please amend the paragraph as follows:

That is, the S71 operator 740 generates the ~~9~~7-bit signal ~~y1~~y0, y2, . . ., y6 by performing parallel logical AND operations and then performing a logical exclusive-OR operation of a 7-bit signal x0, x1, . . ., x6 in parallel. A TR1 unit 730 removes two zeroes from the MSBs of the 9-bit signal RL_1 and outputs the resulting 7-bit signal. A 7-bit signal RR_2 is generated by performing a logical exclusive-OR operation on the outputs of the TR1 730 and the S71 operator 740 with a sub-encryption key $KI_{1,1,1}$. The signal RR_2 is temporarily stored in the first register 800. Upon receipt of a first clock signal CLK1 from a controller (not shown), the register 800 simultaneously outputs the 9-bit signal RL_2 and the 7-bit signal RR_2. Thus the register 800 functions to synchronize the output timings of signals according to delay involved with encryption in the S91 operator 710, the ZE1 unit 720, the TR1 unit 730, and the S71 operator 740.